PATENT COOPERATION TREATY

From the INTERNATIONAL BUREAU

PCT

NOTIFICATION OF ELECTION

(PCT Rule 61.2)

To:

Assistant Commissioner for Patents
United States Patent and Trademark Office
Box PCT
Washington, D.C.20231
ETATS-UNIS D'AMERIQUE

in its capacity as elected Office

Date of mailing: 11 May 2000 (11.05.00)	
International application No.: PCT/EP99/08058	Applicant's or agent's file reference: HL59863/002
International filing date: 25 October 1999 (25.10.99)	Priority date: 30 October 1998 (30.10.98)
Applicant: NAYLOR, Rowan, Nigel	

1. The designated Office is hereby notified of its election made:

[X] in the demand filed with the International preliminary Examining Authority on:

06 March 2000 (06.03.00)

[ ] in a notice effecting later election filed with the International Bureau on:

2. The election [X] was

[ ] was not

made before the expiration of 19 months from the priority date or, where Rule 32 applies, within the time limit under Rule 32.2(b).

The International Bureau of WIPO 34, chemin des Colombettes 1211 Geneva 20, Switzerland Facsimile No.: (41-22) 740.14.35	Authorized officer: J. Zahra Telephone No.: (41-22) 338.83.38

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PATENT COOPERATION TREATY

PCT

INTERNATIONAL PRELIMINARY EXAMINATION REPORT

(PCT Article 36 and Rule 70)

Applicant's or agent's file reference	FOR FURTHER ACTION	See Notification of Transmittal of International Preliminary Examination Report (Form PCT/IPEA/416)
HL59863/002/CIV		
International application No.	International filing date *(day/month/year)*	Priority date *(day/month/year)*
PCT/EP99/08058	25/10/1999	30/10/1998
International Patent Classification (IPC) or national classification and IPC G06F9/38		
Applicant TELEFONAKTIEBOLAGET L M ERICSSON et al.		

1. This international preliminary examination report has been prepared by this International Preliminary Examining Authority and is transmitted to the applicant according to Article 36.

2. This REPORT consists of a total of 7 sheets, including this cover sheet.

   ☒ This report is also accompanied by ANNEXES, i.e. sheets of the description, claims and/or drawings which have been amended and are the basis for this report and/or sheets containing rectifications made before this Authority (see Rule 70.16 and Section 607 of the Administrative Instructions under the PCT).

   These annexes consist of a total of 2 sheets.

3. This report contains indications relating to the following items:

   - I ☒ Basis of the report
   - II ☐ Priority
   - III ☐ Non-establishment of opinion with regard to novelty, inventive step and industrial applicability
   - IV ☐ Lack of unity of invention
   - V ☒ Reasoned statement under Article 35(2) with regard to novelty, inventive step or industrial applicability; citations and explanations suporting such statement
   - VI ☐ Certain documents cited
   - VII ☒ Certain defects in the international application
   - VIII ☒ Certain observations on the international application

Date of submission of the demand	Date of completion of this report
06/03/2000	16.02.2001
Name and mailing address of the international preliminary examining authority: European Patent Office D-80298 Munich Tel. +49 89 2399 - 0 Tx: 523656 epmu d Fax: +49 89 2399 - 4465	Authorized officer Corcoran, P Telephone No. +49 89 2399 2146

Form PCT/IPEA/409 (cover sheet) (January 1994)

INTERNATIONAL PRELIMINARY EXAMINATION REPORT

International application No. PCT/EP99/08058

I. Basis of the r port

1. This report has been drawn on the basis of (*substitute sheets which have been furnished to the receiving Office in response to an invitation under Article 14 are referred to in this report as "originally filed" and are not annexed to the report since they do not contain amendments.*):

Description, pages:

1-8	as originally filed			

Claims, No.:

1-7	as received on	29/09/2000	with letter of	25/09/2000

Drawings, sheets:

1/3-3/3	as originally filed

2. The amendments have resulted in the cancellation of:

☐ the description, pages:
☐ the claims, Nos.:
☐ the drawings, sheets:

3. ☐ This report has been established as if (some of) the amendments had not been made, since they have been considered to go beyond the disclosure as filed (Rule 70.2(c)):

4. Additional observations, if necessary:

V. Reasoned statement under Article 35(2) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement

1. Statement

Novelty (N)	Yes:	Claims	
	No:	Claims	1,6
Inventive step (IS)	Yes:	Claims	2-5
	No:	Claims	7
Industrial applicability (IA)	Yes:	Claims	1-7
	No:	Claims	

2. Citations and explanations

see separate sheet

VII. Certain defects in the international application

The following defects in the form or contents of the international application have been noted:

see separate sheet

VIII. Certain observations on the international application

The following observations on the clarity of the claims, description, and drawings or on the question whether the claims are fully supported by the description, are made:

see separate sheet

V. Reasoned Statement under Article 35(2)

(1) Cited Prior Art

Reference is made to the following documents:

D1: US-A-5 495 588 (KNULL KURT ET AL) 27 February 1996;

D2: GB-A-1 576 276 (SIEMENS AG) 8 October 1980;

D3: US-A-5 283 881 (MARTINI WILLIAM J ET AL) 1 February 1994;

D4: EP-A-0 174 231 (TELEMECANIQUE ELECTRIQUE) 12 March 1986;

D5: W.S. GASS ET AL.: "Multiple digital signal processor environment for intelligent signal processing", PROCEEDINGS OF THE IEEE, NY, USA, September 1987, vol. 75, no. 9, pages 1246 to 1258;

(2) Independent Claims

2.1) Claim 1

D1 discloses a processing arrangement for a computer comprising a first processor means ("general purpose microprocessor") and second processor means ("special processor"), cf. D1: col. 3 l.1-7. The second processor means "may be any other processor optimized for a subset of the instructions to be executed", D1: col.4 l.9-14. This arrangement is understood to be substantially equivalent to arrangement recited in l.1-9 of claim 1, *viz.* the first processor means operable to process instructions from a first set of instructions and second processor means which is operable to process instructions from a second set of instructions, said second set of instructions being a subset of the first set of instructions.

The additional specification of claim 1, *viz.* that the second processor means is *"arranged to receive instructions and to process instructions independently of the first processor means when the received instructions form at least part of the second set of instructions",* is not understood to imply any technical features beyond those of the processing arrangement disclosed in D1.

In view of the foregoing, claim 1 is considered to lack novelty over the disclosure of D1. Moreover, claim 1 fails to define the matter for which protection is sought in terms of its essential technical features as noted in **VIII.** below and even if the novelty of the recited subject matter could be established, no non-obvious technical contribution to the art is evident in the manner in which the claim has been worded.

2.2) Claim 6

Claim 6 recites substantially the same features as claim 1 in the form of a method. Objections corresponding to those raised against claim 1 (cf. **2.1** above) are likewise raised against claim 6 in respect of non-compliance with the provisions of Article 33 PCT.

(3) Dependent Claims

As to claim 2 which is dependent on claim 1, inasmuch as said claim is understood to be directed to the provision of a link between the host and shadow processors described on p.3 l.30 - p.4 l.8, and more specifically to the provision of multiple access to a set of registers by both host and shadow processor via a register bridge unit (cf. p.4 l.32 - p.5 l.2), the subject matter of said claim does not appear to be disclosed or derivable in an obvious manner from the available prior art. In view of the apparent lack of prejudicial disclosure, claims 3-5 insofar as they are dependent on claim 2 can likewise be considered to meet the requirements of Article 33 PCT.

As to claim 7 which is dependent on claim 6, it is known in multiple processing arrangements for instructions to be processed by one processor while another processor is in an inactive (or "suspended") state of operation (cf. D3 Abstract; p.11 l.4-7). Hence, no non-obvious technical contribution to the art is evident in the subject matter of said claim.

VII. Certain Def cts in th Int rnational Application

(1) Contrary to the requirements of Rule 5.1(a)(ii) PCT, the relevant background art disclosed in the documents D1-D5 is not mentioned in the description, nor are these documents identified therein.

(2) Independent claims 1 and 6 are not in the two-part form in accordance with Rule 6.3(b) PCT, which in the present case would be appropriate, with those features known in combination from the prior art (documents D1 and D2) being placed in a preamble (cf. Rule 6.3(b)(i) PCT) and with the remaining features being included in a characterising part (cf. Rule 6.3(b)(ii) PCT).

(3) The features of the claims are not provided with reference signs placed in parentheses (cf. Rule 6.2(b) PCT).

VIII. Certain Observations on the International Application

(1) Claims 1 and 6

1.1) The examiner considers that the present independent claims 1 and 6 do not meet the requirement following from Article 6 PCT taken in combination with Rule 6.3(b) PCT that any independent claim must clearly define the matter for which protection is sought in terms of the technical features essential to the definition of the invention.

1.2) Claim 1

Claim 1 recites a processing arrangement for a computer comprising first and second processor means each operable to process a respective set of instructions, the second set of instructions being a subset of the first set.

The second processor means is *"arranged to receive instructions and to process instructions independently of the first processor means when the received instructions form at least part of the second set of instructions"*.

The cited expression relating to the second processor means lacks clarity for the following reasons.

- The technical features implied by the terms "arranged to receive instructions" and "independently" have not been specified and cannot be clearly determined in the given context.
- Moreover, it is noted that the term "independently" is unacceptably vague in the given context. Given that the description discloses linkages between the

processors in the form of a host interrupt controller and a register bridge unit(19), (cf. p.3 l.30 - p.4 l.8; Fig. 1), it is clear that the "independence" of operation of the second processor with respect to the first is a relative one.

- It is further noted that the mechanism by which the second processor receives instructions has not been specified and therefore the means by which it is determined when the received instructions form at least part of the second set of instructions as stated in the concluding part of the expression remains unclear.

Considered as a whole, the wording of the claim does not amount to more than the statement of a desired result, *viz.* that in a processing arrangement comprising a first and a second processor as recited, the second processor means should be arranged to process received instructions "independently" of the first processor means. Such a definition of subject matter in terms of a result to be achieved does not appear appropriate in the present case (cf. PCT Guidelines III 4.7). Without a more specific definition of the degree of independence envisaged in respect of the operation of the second processor and the technical features required to support it, the matter for which protection is sought cannot be considered to be clearly defined as required by Article 6 PCT.

1.2) Claim 6

Claim 6 recites substantially the same subject matter as claim 1 in the form of a method claim. A corresponding objection due to lack of clarity is raised concerning the wording of claim 6.

(2) Claim 2

Claim 2 is understood to be directed to the provision of a link between the host and shadow processors described on p.3 l.30 - p.4 l.8, and more specifically to the provision of multiple access to a set of registers by both host and shadow processor via a register bridge unit (cf. p.4 l.32 - p.5 l.2). The subject matter of said claim appears to relate to an essential feature of the invention and as such more properly belongs in the independent claims.

CLAIMS

1. A processing arrangement for a computer comprising:

first processor means for processing a first set of instructions; and

second processor means for processing a second set of instructions, the second set of instructions being a subset of the first set of instructions, wherein the second processor means is arranged to receive control signals and to process instructions in dependence upon those control signals without reference to the first processor means.

2. An arrangement as claimed in claim 1, wherein the first processor means includes a plurality of registers, and the second processor means has access to a predetermined selection of the said registers.

3. An arrangement as claimed in claim 1 or 2, wherein the first processor means has active and inactive states of operation, and wherein the second processor means is operable to process instructions when the first processor means is in the inactive state.

4. An arrangement as claimed in claim 3, wherein the second processor means is operable to cause the first processor means to change to the active state from the inactive state, when received control signals are indicative of instructions which cannot be processed by the second processor means.

5. A method of operating a computer including first processor means for processing a first set of instructions, and second processor means for processing a second set of instructions, the second set of instructions being a subset of the first set of instructions, the method comprising:

using the second processor means to receive

control signals; and

processing instructions in dependence upon the received control signals using the second processor means without reference to the first processor means when the received control signals are part of said second set of instructions.

6. A method as claimed in claim 5, wherein the first processor means has active and inactive states of operation, and instructions are processed using the second processor means when the first processor means is in the inactive state if they are part of said second set.

7. A processing arrangement for a computer, comprising first and second processors, the second processor being code compatible with the first processor, such that instruction code can be shared between the first and second processors and can be operated on by the first or second processor without the need for conversion or alteration.

8. A processing arrangement for a computer comprising a plurality of processing elements, each element being assigned a predetermined function, wherein the processing elements are able to share instruction code without conversion or alteration, and the plurality of elements provides functionality equivalent to a predetermined virtual processor.

CLAIMS

1. A processing arrangement for a computer, the arrangement comprising:

first processor means which is operable to process instructions from a first set of instructions; and

second processor means which is operable to process instructions from a second set of instructions, which second set of instructions is a subset of the first set of instructions, the second processor means being arranged to receive instructions and to process the received instructions independently of the first processor means, when the received instructions form at least part of the second set of instructions.

2. An arrangement as claimed in claim 1, wherein the first processor means includes a plurality of registers, and the second processor means is operable to access a predetermined selection of the said registers.

3. An arrangement as claimed in claims 1 or 2 , wherein the first processor means has active and inactive states of operation, and wherein the second processor means is operable to process instructions when the first processor means is in the inactive state.

4. An arrangement as claimed in claim 3, wherein the second processor means is operable to cause the first processor means to change to the active state from the inactive state, when the received instructions cannot be processed by the second processor means.

5. A processing arrangement as claimed in any one of claims 1 to 4, comprising a plurality of such second processor means for processing respective subsets of the first instruction set.

6. A method of operating a computer including first processor means which operates to process instructions from a first set of instructions, and

second processor means which operates to process instructions from a second set of instructions, which second set of instructions is a subset of the first set of instructions, the method comprising:

using the second processor means to receive instructions; and

processing the received instructions using the second processor means independently of the first processor means when the received instructions form at least a part of said second set of instructions.

7. A method as claimed in claim 6, wherein the first processor means has active and inactive states of operation, and instructions are processed using the second processor means when the first processor means is in the inactive state of operation.

PATENT COOPERATION TREATY

PCT

INTERNATIONAL SEARCH REPORT

(PCT Article 18 and Rules 43 and 44)

Applicant's or agent's file reference	**FOR FURTHER ACTION** see Notification of Transmittal of International Search Report (Form PCT/ISA/220) as well as, where applicable, item 5 below.	
HL59863/002		
International application No.	International filing date *(day/month/year)*	(Earliest) Priority Date *(day/month/year)*
PCT/EP 99/08058	25/10/1999	30/10/1998
Applicant		
TELEFONAKTIEBOLAGET L M ERICSSON et al.		

This International Search Report has been prepared by this International Searching Authority and is transmitted to the applicant according to Article 18. A copy is being transmitted to the International Bureau.

This International Search Report consists of a total of 3 sheets.

[X] It is also accompanied by a copy of each prior art document cited in this report.

1. **Basis of the report**

   a. With regard to the **language,** the international search was carried out on the basis of the international application in the language in which it was filed, unless otherwise indicated under this item.

   [ ] the international search was carried out on the basis of a translation of the international application furnished to this Authority (Rule 23.1(b)).

   b. With regard to any **nucleotide and/or amino acid sequence** disclosed in the international application, the international search was carried out on the basis of the sequence listing :

   [ ] contained in the international application in written form.

   [ ] filed together with the international application in computer readable form.

   [ ] furnished subsequently to this Authority in written form.

   [ ] furnished subsequently to this Authority in computer readble form.

   [ ] the statement that the subsequently furnished written sequence listing does not go beyond the disclosure in the international application as filed has been furnished.

   [ ] the statement that the information recorded in computer readable form is identical to the written sequence listing has been furnished

2. [ ] **Certain claims were found unsearchable** (See Box I).

3. [ ] **Unity of invention is lacking** (see Box II).

4. With regard to the **title,**

   [X] the text is approved as submitted by the applicant.

   [ ] the text has been established by this Authority to read as follows:

5. With regard to the **abstract,**

   [X] the text is approved as submitted by the applicant.

   [ ] the text has been established, according to Rule 38.2(b), by this Authority as it appears in Box III. The applicant may, within one month from the date of mailing of this international search report, submit comments to this Authority.

6. The figure of the **drawings** to be published with the abstract is Figure No. 1

   [X] as suggested by the applicant.

   [ ] because the applicant failed to suggest a figure.

   [ ] because this figure better characterizes the invention.

   [ ] None of the figures.

INTERNATIONAL SEARCH REPORT

International Application No
P[redacted]P 99/08058

A. CLASSIFICATION OF SUBJECT MATTER
IPC 7 G06F9/38

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 7 G06F

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 5 495 588 A (KNULL KURT ET AL) 27 February 1996 (1996-02-27) column 2, line 35 -column 3, line 18 column 4, line 3 - line 11 column 4, line 56 - line 65 column 5, line 66 -column 6, line 2	1,3-8
X	GB 1 576 276 A (SIEMENS AG) 8 October 1980 (1980-10-08)	1,3,5,7, 8
A	the whole document	4
A	US 5 283 881 A (MARTINI WILLIAM J ET AL) 1 February 1994 (1994-02-01) column 3, line 40 - line 48	2

-/--

[X] Further documents are listed in the continuation of box C.

[X] Patent family members are listed in annex.

° Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier document but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
31 January 2000	04/02/2000

Name and mailing address of the ISA	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL – 2280 HV Rijswijk Tel. (+31–70) 340–2040, Tx. 31 651 epo nl, Fax: (+31–70) 340–3016	Moraiti, M

1

Form PCT/ISA/210 (second sheet) (July 1992)

INTERNATIONAL SEARCH REPORT

International Application No
P[redacted]P 99/08058

C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication,where appropriate, of the relevant passages	Relevant to claim No.
A	EP 0 174 231 A (TELEMECANIQUE ELECTRIQUE) 12 March 1986 (1986-03-12) page 6, line 5 -page 7, line 34 page 11, line 4 -page 12, line 2	1,3-8

Form PCT/ISA/210 (continuation of second sheet) (July 1992)

INTERNATIONAL SEARCH REPORT

Information on patent family members

International Application No
P[redacted]EP 99/08058

Patent document cited in search report		Publication date	Patent family member(s)		Publication date
US 5495588	A	27-02-1996	NONE		
GB 1576276	A	08-10-1980	DE	2607685 A	01-09-1977
			AT	353363 B	12-11-1979
			AT	50677 A	15-04-1979
			BE	851840 A	25-08-1977
			CH	610122 A	30-03-1979
			FR	2342530 A	23-09-1977
			IT	1078233 B	08-05-1985
			NL	7701537 A	29-08-1977
US 5283881	A	01-02-1994	NONE		
EP 0174231	A	12-03-1986	US	4716541 A	29-12-1987
			CA	1234223 A	15-03-1988
			CA	1233258 A	23-02-1988
			EP	0174230 A	12-03-1986
			US	4870614 A	26-09-1989

PATENT COOPERATION TREATY

From the
INTERNATIONAL PRELIMINARY EXAMINING AUTHORITY

To:

VIGARS, Christopher Ian
HASELTINE LAKE & CO.
Imperial House
15-19 Kingsway
London WC2B 6UD
GRANDE BRETAGNE

PCT

NOTIFICATION OF TRANSMITTAL OF
THE INTERNATIONAL PRELIMINARY
EXAMINATION REPORT
(PCT Rule 71.1)

Date of mailing *(day/month/year)*	16.02.2001
Applicant's or agent's file reference HL59863/002/CIV	**IMPORTANT NOTIFICATION**

International application No.	International filing date *(day/month/year)*	Priority date *(day/month/year)*
PCT/EP99/08058	25/10/1999	30/10/1998

Applicant
TELEFONAKTIEBOLAGET L M ERICSSON et al.

1. The applicant is hereby notified that this International Preliminary Examining Authority transmits herewith the international preliminary examination report and its annexes, if any, established on the international application.

2. A copy of the report and its annexes, if any, is being transmitted to the International Bureau for communication to all the elected Offices.

3. Where required by any of the elected Offices, the International Bureau will prepare an English translation of the report (but not of any annexes) and will transmit such translation to those Offices.

4. **REMINDER**

The applicant must enter the national phase before each elected Office by performing certain acts (filing translations and paying national fees) within 30 months from the priority date (or later in some Offices) (Article 39(1)) (see also the reminder sent by the International Bureau with Form PCT/IB/301).

Where a translation of the international application must be furnished to an elected Office, that translation must contain a translation of any annexes to the international preliminary examination report. It is the applicant's responsibility to prepare and furnish such translation directly to each elected Office concerned.

For further details on the applicable time limits and requirements of the elected Offices, see Volume II of the PCT Applicant's Guide.

Name and mailing address of the IPEA/	Authorized officer
European Patent Office D-80298 Munich Tel. +49 89 2399 - 0 Tx: 523656 epmu d Fax: +49 89 2399 - 4465	Camps i Amigo, M.E. Tel.+49 89 2399-2237

Form PCT/IPEA/416 (July 1992)

PATENT COOPERATION TREATY

PCT

INTERNATIONAL PRELIMINARY EXAMINATION REPORT

(PCT Article 36 and Rule 70)

Applicant's or agent's file reference	FOR FURTHER ACTION	See Notification of Transmittal of International Preliminary Examination Report (Form PCT/IPEA/416)
HL59863/002/CIV		
International application No.	International filing date *(day/month/year)*	Priority date *(day/month/year)*
PCT/EP99/08058	25/10/1999	30/10/1998
International Patent Classification (IPC) or national classification and IPC G06F9/38		
Applicant TELEFONAKTIEBOLAGET L M ERICSSON et al.		

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3. This report contains indications relating to the following items:

   - I ☒ Basis of the report
   - II ☐ Priority
   - III ☐ Non-establishment of opinion with regard to novelty, inventive step and industrial applicability
   - IV ☐ Lack of unity of invention
   - V ☒ Reasoned statement under Article 35(2) with regard to novelty, inventive step or industrial applicability; citations and explanations suporting such statement
   - VI ☐ Certain documents cited
   - VII ☒ Certain defects in the international application
   - VIII ☒ Certain observations on the international application

Date of submission of the demand	Date of completion of this report
06/03/2000	16.02.2001
Name and mailing address of the international preliminary examining authority: European Patent Office D-80298 Munich Tel. +49 89 2399 - 0 Tx: 523656 epmu d Fax: +49 89 2399 - 4465	Authorized officer Corcoran, P Telephone No. +49 89 2399 2146

Form PCT/IPEA/409 (cover sheet) (January 1994)

INTERNATIONAL PRELIMINARY EXAMINATION REPORT

International application No. PCT/EP99/08058

I. Basis of the report

1. This report has been drawn on the basis of (*substitute sheets which have been furnished to the receiving Office in response to an invitation under Article 14 are referred to in this report as "originally filed" and are not annexed to the report since they do not contain amendments.*):

Description, pages:

1-8	as originally filed

Claims, No.:

1-7	as received on	29/09/2000	with letter of	25/09/2000

Drawings, sheets:

1/3-3/3	as originally filed

2. The amendments have resulted in the cancellation of:

- ☐ the description, pages:
- ☐ the claims, Nos.:
- ☐ the drawings, sheets:

3. ☐ This report has been established as if (some of) the amendments had not been made, since they have been considered to go beyond the disclosure as filed (Rule 70.2(c)):

4. Additional observations, if necessary:

V. Reasoned statement under Article 35(2) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement

1. Statement

Novelty (N)	Yes:	Claims	
	No:	Claims	1,6
Inventive step (IS)	Yes:	Claims	2-5
	No:	Claims	7
Industrial applicability (IA)	Yes:	Claims	1-7
	No:	Claims	

2. Citations and explanations

see separate sheet

VII. Certain defects in the international application

The following defects in the form or contents of the international application have been noted:

see separate sheet

VIII. Certain observations on the international application

The following observations on the clarity of the claims, description, and drawings or on the question whether the claims are fully supported by the description, are made:

see separate sheet

V. Reason d Statement und r Articl 35(2)

(1) Cited Prior Art

Reference is made to the following documents:

D1: US-A-5 495 588 (KNULL KURT ET AL) 27 February 1996;

D2: GB-A-1 576 276 (SIEMENS AG) 8 October 1980;

D3: US-A-5 283 881 (MARTINI WILLIAM J ET AL) 1 February 1994;

D4: EP-A-0 174 231 (TELEMECANIQUE ELECTRIQUE) 12 March 1986;

D5: W.S. GASS ET AL.: "Multiple digital signal processor environment for intelligent signal processing", PROCEEDINGS OF THE IEEE, NY, USA, September 1987, vol. 75, no. 9, pages 1246 to 1258;

(2) Independent Claims

2.1) Claim 1

D1 discloses a processing arrangement for a computer comprising a first processor means ("general purpose microprocessor") and second processor means ("special processor"), cf. D1: col. 3 l.1-7. The second processor means "may be any other processor optimized for a subset of the instructions to be executed", D1: col.4 l.9-14. This arrangement is understood to be substantially equivalent to arrangement recited in l.1-9 of claim 1, *viz.* the first processor means operable to process instructions from a first set of instructions and second processor means which is operable to process instructions from a second set of instructions, said second set of instructions being a subset of the first set of instructions.

The additional specification of claim 1, *viz.* that the second processor means is *"arranged to receive instructions and to process instructions independently of the first processor means when the received instructions form at least part of the second set of instructions",* is not understood to imply any technical features beyond those of the processing arrangement disclosed in D1.

In view of the foregoing, claim 1 is considered to lack novelty over the disclosure of D1. Moreover, claim 1 fails to define the matter for which protection is sought in terms of its essential technical features as noted in **VIII.** below and even if the novelty of the recited subject matter could be established, no non-obvious technical contribution to the art is evident in the manner in which the claim has been worded.

2.2) Claim 6

Claim 6 recites substantially the same features as claim 1 in the form of a method. Objections corresponding to those raised against claim 1 (cf. **2.1** above) are likewise raised against claim 6 in respect of non-compliance with the provisions of Article 33 PCT.

(3) Dependent Claims

As to claim 2 which is dependent on claim 1, inasmuch as said claim is understood to be directed to the provision of a link between the host and shadow processors described on p.3 l.30 - p.4 l.8, and more specifically to the provision of multiple access to a set of registers by both host and shadow processor via a register bridge unit (cf. p.4 l.32 - p.5 l.2), the subject matter of said claim does not appear to be disclosed or derivable in an obvious manner from the available prior art. In view of the apparent lack of prejudicial disclosure, claims 3-5 insofar as they are dependent on claim 2 can likewise be considered to meet the requirements of Article 33 PCT.

As to claim 7 which is dependent on claim 6, it is known in multiple processing arrangements for instructions to be processed by one processor while another processor is in an inactive (or "suspended") state of operation (cf. D3 Abstract; p.11 l.4-7). Hence, no non-obvious technical contribution to the art is evident in the subject matter of said claim.

VII. Certain Defects in the International Application

(1) Contrary to the requirements of Rule 5.1(a)(ii) PCT, the relevant background art disclosed in the documents D1-D5 is not mentioned in the description, nor are these documents identified therein.

(2) Independent claims 1 and 6 are not in the two-part form in accordance with Rule 6.3(b) PCT, which in the present case would be appropriate, with those features known in combination from the prior art (documents D1 and D2) being placed in a preamble (cf. Rule 6.3(b)(i) PCT) and with the remaining features being included in a characterising part (cf. Rule 6.3(b)(ii) PCT).

(3) The features of the claims are not provided with reference signs placed in parentheses (cf. Rule 6.2(b) PCT).

VIII. Certain Observations on the International Application

(1) Claims 1 and 6

1.1) The examiner considers that the present independent claims 1 and 6 do not meet the requirement following from Article 6 PCT taken in combination with Rule 6.3(b) PCT that any independent claim must clearly define the matter for which protection is sought in terms of the technical features essential to the definition of the invention.

1.2) Claim 1

Claim 1 recites a processing arrangement for a computer comprising first and second processor means each operable to process a respective set of instructions, the second set of instructions being a subset of the first set.

The second processor means is *"arranged to receive instructions and to process instructions independently of the first processor means when the received instructions form at least part of the second set of instructions"*.

The cited expression relating to the second processor means lacks clarity for the following reasons.

- The technical features implied by the terms "arranged to receive instructions" and "independently" have not been specified and cannot be clearly determined in the given context.
- Moreover, it is noted that the term "independently" is unacceptably vague in the given context. Given that the description discloses linkages between the

processors in the form of a host interrupt controller and a register bridge unit(19), (cf. p.3 l.30 - p.4 l.8; Fig. 1), it is clear that the "independence" of operation of the second processor with respect to the first is a relative one.

- It is further noted that the mechanism by which the second processor receives instructions has not been specified and therefore the means by which it is determined when the received instructions form at least part of the second set of instructions as stated in the concluding part of the expression remains unclear.

Considered as a whole, the wording of the claim does not amount to more than the statement of a desired result, *viz.* that in a processing arrangement comprising a first and a second processor as recited, the second processor means should be arranged to process received instructions "independently" of the first processor means. Such a definition of subject matter in terms of a result to be achieved does not appear appropriate in the present case (cf. PCT Guidelines III 4.7). Without a more specific definition of the degree of independence envisaged in respect of the operation of the second processor and the technical features required to support it, the matter for which protection is sought cannot be considered to be clearly defined as required by Article 6 PCT.

1.2) Claim 6

Claim 6 recites substantially the same subject matter as claim 1 in the form of a method claim. A corresponding objection due to lack of clarity is raised concerning the wording of claim 6.

(2) Claim 2

Claim 2 is understood to be directed to the provision of a link between the host and shadow processors described on p.3 l.30 - p.4 l.8, and more specifically to the provision of multiple access to a set of registers by both host and shadow processor via a register bridge unit (cf. p.4 l.32 - p.5 l.2). The subject matter of said claim appears to relate to an essential feature of the invention and as such more properly belongs in the independent claims.

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(71) Applicant *(for all designated States except US)*: TELEFONAKTIEBOLAGET LM ERICSSON [SE/SE]; S–126 25 Stockholm (SE).

(72) Inventor; and

(75) Inventor/Applicant *(for US only)*: NAYLOR, Rowan, Nigel [GB/GB]; 4 Lisa Court, Downsland Road, Basingstoke RG21 1TU (GB).

(74) Agent: VIGARS, Christopher, Ian; Haseltine Lake & Co., Imperial House, 15–19 Kingsway, London WC2B 6UD (GB).

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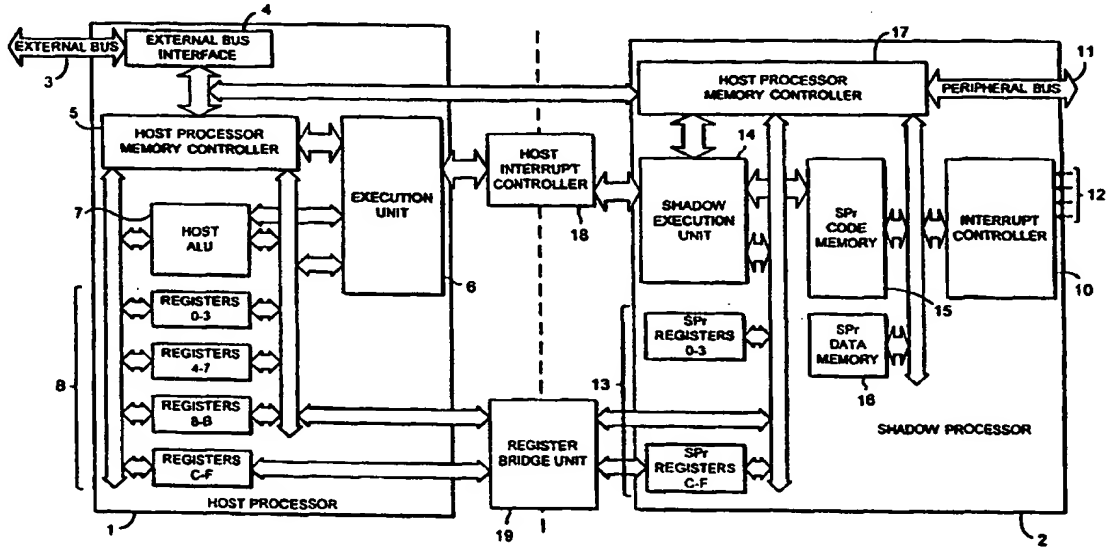

(57) Abstract

A processing arrangement for a computer comprising: first processor means (1) for processing a first set of instructions; and second processor means (2) for processing a second set of instructions, the second set of instructions being a subset of the first set of instructions, wherein the second processor means (2) is arranged to receive control signals and to process instructions in dependence upon those control signals without reference to the first processor means.

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PROCESSING ARRANGEMENTS

The present invention relates to processing arrangements for computer architectures.

DESCRIPTION OF THE RELATED ART

There are many conventional computer architectures which are based on a single main processor cooperating with a co-processor. The co-processor adds functionality that the main processor in the architecture does not have or does not perform particularly efficiently. The co-processor generally uses instructions which are not implemented in the instruction set of the main processor. As such, many co-processors are used to address very specific code requirements, for example floating point arithmetic or signal processing. In most applications, this means that the instruction set of the co-processor is specific to that co-processor.

In addition, many main processors use real time operating systems to service multiple tasks and exceptions, such as interrupts. Servicing multiple tasks can result in context changes which can absorb significant amounts of the processing power available in the processor. A context change occurs when the task being executed by a processor is changed. The context of a task relates to the code corresponding to the task, and the state of the internal registers of the processor. Furthermore, in low power applications, in order to conserve power, sleep modes are used from which the processor must be reactivated when interrupt or service requests occur. When the processor is reactivated the context must be loaded and then the service performed, the processor then returns to an inactive state. Such a process can consume a large amount of power.

It is therefore desirable to provide a computer

architecture which can overcome these disadvantages.

SUMMARY OF THE PRESENT INVENTION

According to one aspect of the present invention there is provided a processing arrangement for a computer comprising:

first processor means for processing a first set of instructions; and

second processor means for processing a second set of instructions, the second set of instructions being a subset of the first set of instructions, wherein the second processor means is arranged to receive control signals and to process instructions in dependence upon those control signals without reference to the first processor means.

BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1 is a block diagram illustrating a computer processor architecture in accordance with the present invention;

Figure 2 shows a computer architecture including multiple processors; and

Figure 3 is a diagramatic illustration of how processors embodying the present invention can realise the functionality of a desired virtual processor.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

Figure 1 shows a block diagram illustrating a host (or first) processor 1 connected with a shadow (or second) processor 2. In the example shown, the shadow processor 2 is used to control interrupts received from peripherals connected to the processor system.

The host processor 1 communicates with an external bus 3 by way of an external bus interface 4. The external bus 3 is used for transferring data to and from the main processor and memory devices (not shown).

The host processor 1 also includes a memory controller 5 for controlling data access with memory devices. The memory controller 5 is controlled itself by an execution unit 6 which has overall control of the main processor 1. The host processor 1 also include an arithmetic logic unit (ALU) 7 and a number of registers 8, sixteen in the example shown. The various components of the host processor 1 communicate with each other by way of appropriate internal buses.

In order that the host processor 1 can be held in a low power inactive mode for as long as possible, a shadow processor 2 is connected to the main processor 1. The shadow processor 2 includes an interrupt controller 10 which receives interrupt signals via interrupt inputs 12. The shadow processor also includes registers which correspond to selected ones of the registers of the host processor 1. The interrupt controller can be connected, as in the example of Figure 1, to peripherals connected to a peripheral bus 11.

The shadow processor 2 also includes an execution unit 14, code memory 15, and data memory 16. The shadow processor 2 operates to process a selected subset of the instructions from which the host processor operates, and these instructions are stored in the code memory 15. The shadow processor 2 has access to the host processor memory by way of a memory controller 17 which interfaces with the external bus 3 by way of the host external bus interface 4.

In order to provide a link between the host processor 1 and the shadow processor 2, the execution units of the two processors are connected by way of a host interrupt controller 18, and the registers of the processors are connected by a register bridge unit 19. The Host Interrupt Controller 18 is a module which

allows the shadow processor to issue an interrupt to the host porcessor in order to cause a change in task execution, a context change, appropriate to the requirements of the system. It generates an interrupt to the host using the host interrupt protocol and indicating the source of the interrupt as a vector programmed by the shadow process related to the new task required.

The following description, of the process used to service an interrupt received from a peripheral bus 11 is one example of the operation of the shadow processor 2. A peripheral (not shown) raises an interrupt request on the interrupt input lines 12. The input controller 10 operates to interpret the interrupt request, and if the interrupt request is of the type able to be processed by the shadow processor 2, then the shadow processor 2 will service that interrupt. An example of an interrupt is if an external device such as a serial port has received data from a system to which it is attached. The data from such a serial port may be contained within a message body including information about the source and content of the data. The shadow processor 2 then services the interrupts required by receiving the message then removing the data from that message. Once the data has been removed and checked it issues an interrupt to the main processor 1 via the Host Interrupt Contoller 18 having first set up the context needed by the task to service the data within the message. The main processor 1 would begin processing the data while the shadow processor 2 stores the context of the interrupted task.

The Register Bridge unit 19 allows multiple access to a set of registers by both host and shadow processor. It allows physical registers to appear in both processor systems while resolving any conflict in

their access and mapping of those registers within the physical resource space of the processors.

This unit contains multiplexers to allow dual access to either processor buses, arbitration logic to prevent access conflict, and logic to allow access addresses to be altered to allow re-mapping of the location of the registers in the address map of either processor.

For example registers mapped to positions 4-7 in the host may appear also in positions 4-7 in the shadow or be re-mapped to 8-11 of the shadow. Or in the case of register swapping, registers x-y of the host may be exchanged for equivalent registers in the shadow and vice-versa. This allows registers x-y of the shadow to be loaded with a new context then swapped in to the host in a context change. The registers replaced in the shadow would contain the old host context and can be stored or re-stored by the shadow while the host is processing the new context.

While the host processor 1 is processing a task or is in an unactive ("sleep") mode, the shadow processor 2 will accept interrupts to determine the requirement and decide on the action required. If the action can be handled by the shadow processor alone then it is serviced without reference to the host, but if it does require some intervention by the host, the shadow processor 2 will activate the host processor by way of the host interrupt controller 18.

In the example shown, the shadow processor 2 can service routine requests from the peripherals without the need for host intervention. Data to be processed is shared between the host processor and the shadow processor by way of the register bridge unit 19, in order that the same data can be operated on by both processors.

It will be readily appreciated that, the shadow processor 2 is able to use a subset of the instruction set of the host processor. The main advantage of such a shadow processor is that instruction code can be readily shared between the host and the shadow, without the need for processor emulation or complex code conversion. The other significant advantage is that any work needed to develop the shadow processor can be based on the host processor development work. In addition, the shadow processor design can be optimised, based specifically on the processing of a limited range of instructions of the host processor. Code written for such an application can be analysed to identify the most frequently used instructions, and shadow processors can be provided for those most frequently used instructions. The shadow processor can then be based on the common instruction set but minimum register and addressing range requirements. The shadow processor has access to all the relevant register and memory areas used by the host processor and so the host and shadow processor can work in tandem, the shadow processor performing tasks for which it is designed independently of any reference to the host processor. It will be appreciated that a plurality of shadow processors can be used with a single host processor to provide efficient data processing without the need to refer directly to the host processor itself.

One particular advantage of such system is that the shadow processor can service interrupt requests and other routine tasks without the need to move the host processor into an active state. This can reduce the power consumption of the processing system in total.

It will be appreciated that it is possible to provide all of the functionality of a single host processor by a plurality of shadow processors each

dedicated to a single part of that functionality of the host processor. In this way it is possible to produce a processing architecture which does not need to use a host processor as such, but can use a group of shadow processors each of which is optimised for a particular function. Such architectures are illustrated in Figures 2 and 3, which show that shadow processors can be arranged to share data and registers so that processing of program steps can have continuity.

Figure 2 is an application of a shadow processor concept without the use of a host processor.

A number of shadow processors are arranged in sequence; each processor performs a particular process on data derived from previous shadow processors and passes the processed data on to the next in the sequence. The sequence has input/output ports on the end shadow processors for connection to other system components. Processing occurs in both directions from shadow processor (i.e. 1 to 5 and 5 to 1). In addition sections 3 and 4 contain two shadow processors (A&B) with additional input/output to be combined with the main sequence. Shadow processor 6 performs the task of memory control and ensures that appropriate code is loaded into the shadow processors from main memory as required. It also performs the main co-ordination task for the system.

An application is of such a configuration could be a telecommunications terminal. The I/O of shadow processor 1 would be attached to the RF subsystem, I/O of processor 5 to the Audio sub-system. The secondary I/O of shadow processors 3b/4b to the data processing, and user interfaces e.g. LCD and keyboard. Each of the shadow processors 1-5 perform specific tasks required such as audio codec, interleaving/de-interleaving, etc.

Figure 3 is an example of a virtual processor

concept.

The main processor is provided as a virtual processor, which may only exist in concept and as a simulation. From this virtual processor various applications are analysed and specific implementations derived. Three such implementations 1-3 are drawn below the Host. Each of the implementations contains specific components of the host required by the applications. For example, Shadow processor A. (1) could be characteristic of a RISC CPU, Shadow processor B (2) could be an example of a logic processor, and Shadow processor C (3) could be an example of a memory management processor.

The important distinction of figure 3 is that the host is a virtual processor it may not physically exist.

The shadow processors are optimised fragments of the virtual processor synthesised to a physical implementation on a chip.

CLAIMS

1. A processing arrangement for a computer comprising:

first processor means for processing a first set of instructions; and

second processor means for processing a second set of instructions, the second set of instructions being a subset of the first set of instructions, wherein the second processor means is arranged to receive control signals and to process instructions in dependence upon those control signals without reference to the first processor means.

2. An arrangement as claimed in claim 1, wherein the first processor means includes a plurality of registers, and the second processor means has access to a predetermined selection of the said registers.

3. An arrangement as claimed in claim 1 or 2, wherein the first processor means has active and inactive states of operation, and wherein the second processor means is operable to process instructions when the first processor means is in the inactive state.

4. An arrangement as claimed in claim 3, wherein the second processor means is operable to cause the first processor means to change to the active state from the inactive state, when received control signals are indicative of instructions which cannot be processed by the second processor means.

5. A method of operating a computer including first processor means for processing a first set of instructions, and second processor means for processing a second set of instructions, the second set of instructions being a subset of the first set of instructions, the method comprising:

using the second processor means to receive

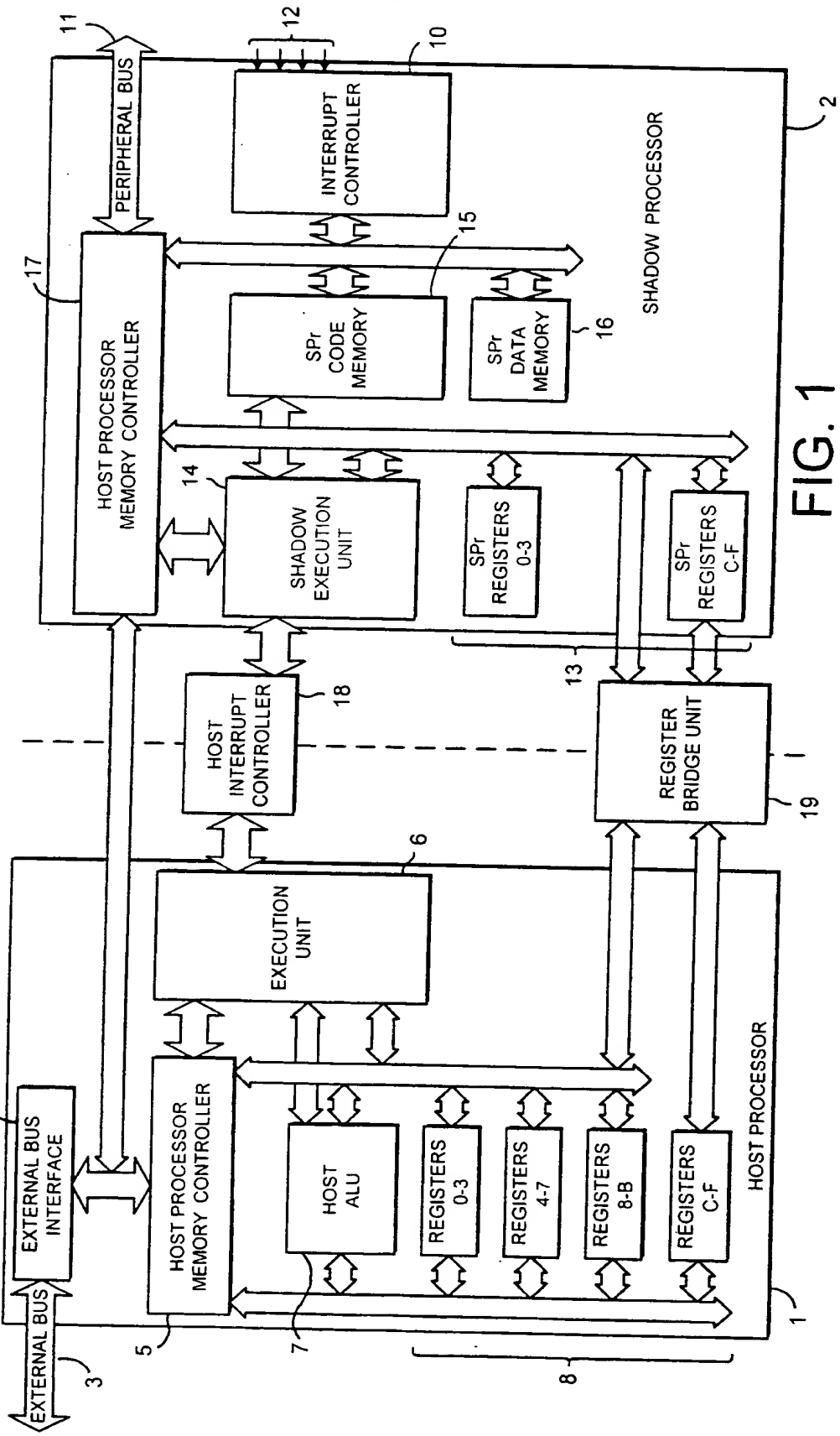
control signals; and

processing instructions in dependence upon the received control signals using the second processor means without reference to the first processor means when the received control signals are part of said second set of instructions.

6. A method as claimed in claim 5, wherein the first processor means has active and inactive states of operation, and instructions are processed using the second processor means when the first processor means is in the inactive state if they are part of said second set.

7. A processing arrangement for a computer, comprising first and second processors, the second processor being code compatible with the first processor, such that instruction code can be shared between the first and second processors and can be operated on by the first or second processor without the need for conversion or alteration.

8. A processing arrangement for a computer comprising a plurality of processing elements, each element being assigned a predetermined function, wherein the processing elements are able to share instruction code without conversion or alteration, and the plurality of elements provides functionality equivalent to a predetermined virtual processor.


EXTERNAL BUS
EXTERNAL BUS INTERFACE
HOST PROCESSOR MEMORY CONTROLLER
HOST ALU
REGISTERS 0-3
REGISTERS 4-7
REGISTERS 8-B
REGISTERS C-F
HOST PROCESSOR
EXECUTION UNIT
HOST INTERRUPT CONTROLLER
REGISTER BRIDGE UNIT
SHADOW EXECUTION UNIT
SPr REGISTERS 0-3
SPr REGISTERS C-F
HOST PROCESSOR MEMORY CONTROLLER
SPr CODE MEMORY
SPr DATA MEMORY
SHADOW PROCESSOR
INTERRUPT CONTROLLER
PERIPHERAL BUS
1
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10
11
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14
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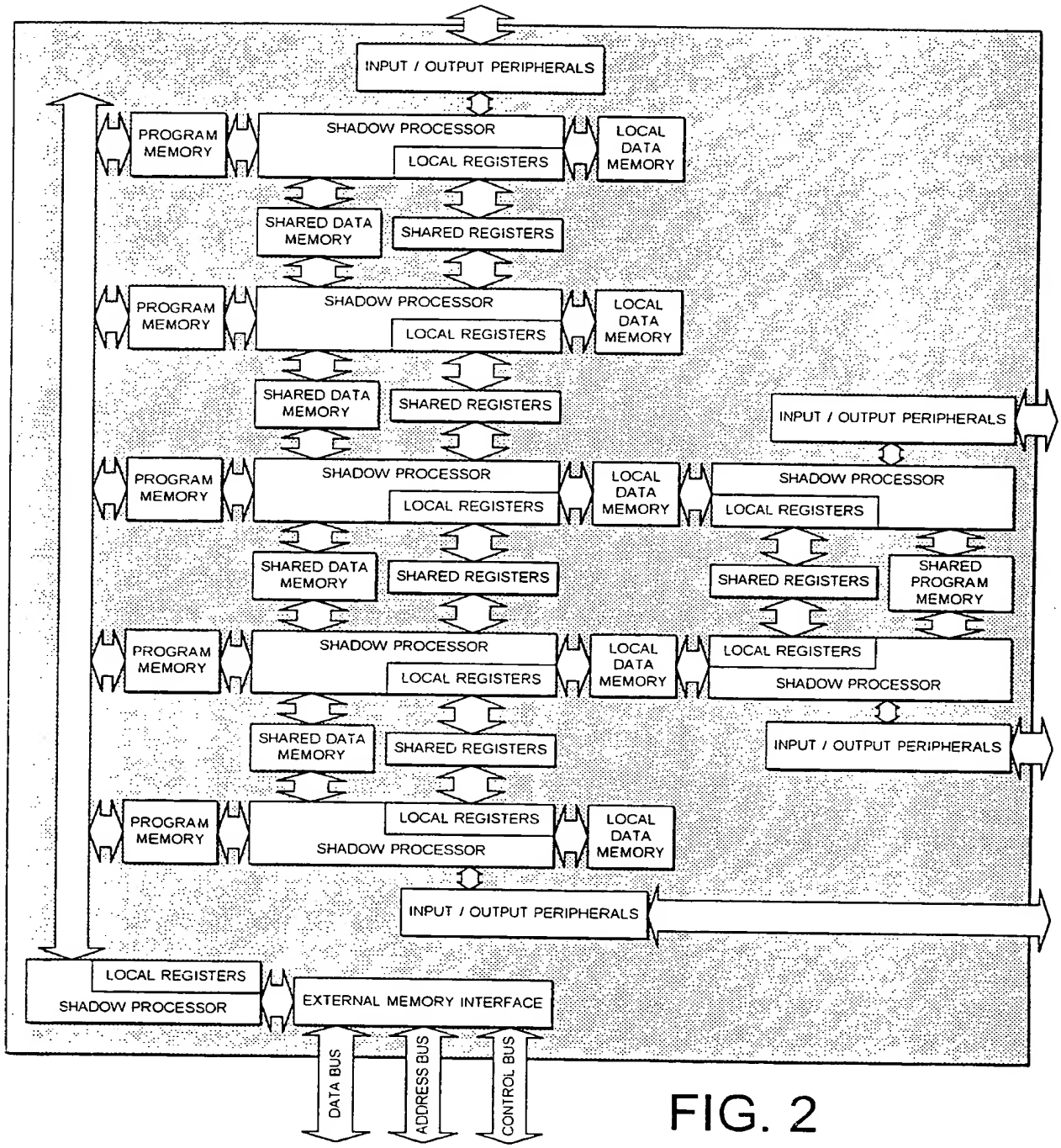
16
17
18
19

FIG. 1


INPUT / OUTPUT PERIPHERALS
PROGRAM MEMORY
SHADOW PROCESSOR
LOCAL REGISTERS
LOCAL DATA MEMORY
SHARED DATA MEMORY
SHARED REGISTERS
PROGRAM MEMORY
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LOCAL REGISTERS
LOCAL DATA MEMORY
SHARED DATA MEMORY
SHARED REGISTERS
INPUT / OUTPUT PERIPHERALS
PROGRAM MEMORY
SHADOW PROCESSOR
LOCAL REGISTERS
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PROGRAM MEMORY
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SHARED DATA MEMORY
SHARED REGISTERS
INPUT / OUTPUT PERIPHERALS
PROGRAM MEMORY
LOCAL REGISTERS
SHADOW PROCESSOR
LOCAL DATA MEMORY
INPUT / OUTPUT PERIPHERALS
LOCAL REGISTERS
SHADOW PROCESSOR
EXTERNAL MEMORY INTERFACE
DATA BUS
ADDRESS BUS
CONTROL BUS

FIG. 2

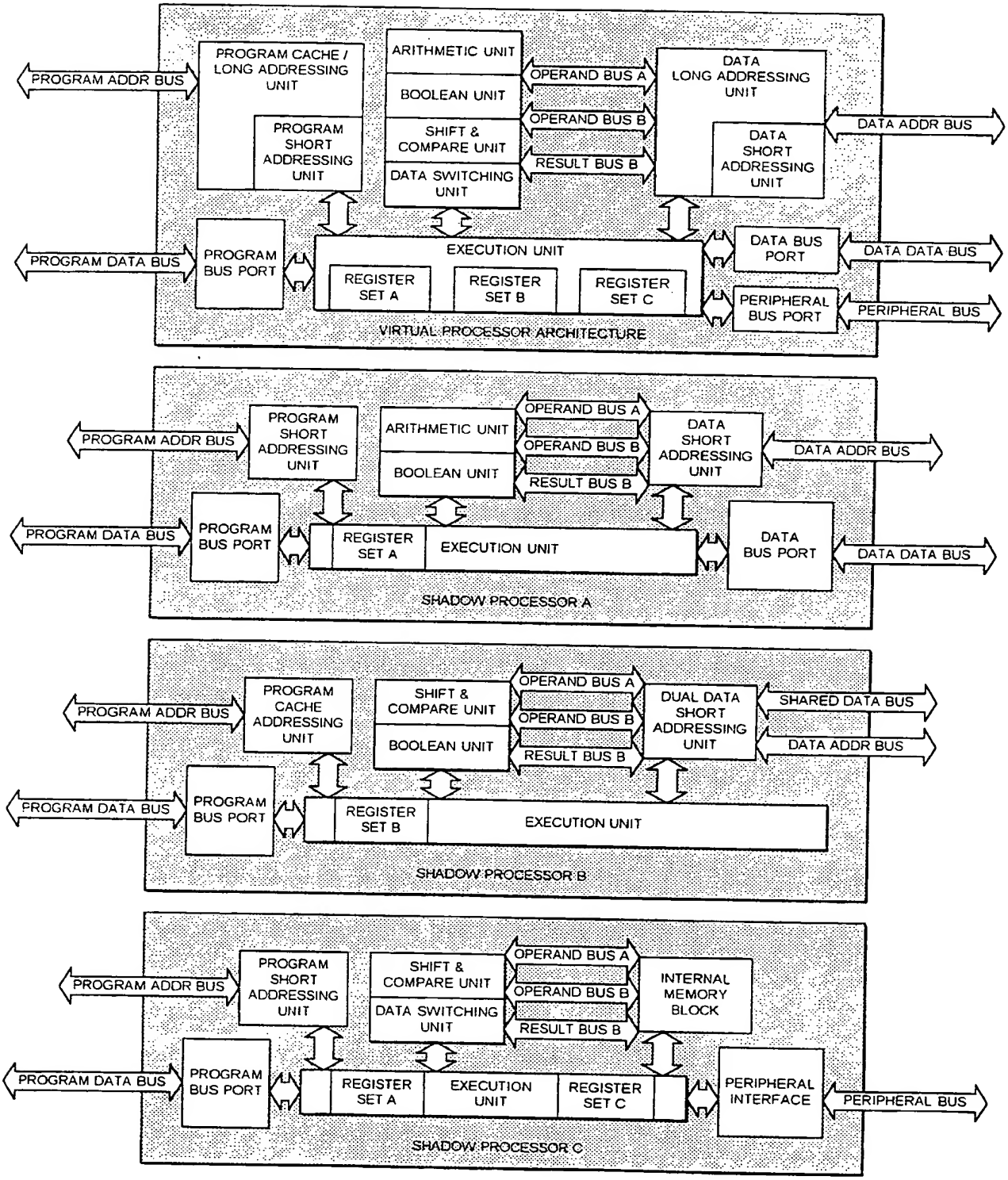
PROGRAM ADDR BUS
PROGRAM CACHE / LONG ADDRESSING UNIT
PROGRAM SHORT ADDRESSING UNIT
ARITHMETIC UNIT
BOOLEAN UNIT
SHIFT & COMPARE UNIT
DATA SWITCHING UNIT
OPERAND BUS A
OPERAND BUS B
RESULT BUS B
DATA LONG ADDRESSING UNIT
DATA SHORT ADDRESSING UNIT
DATA ADDR BUS
PROGRAM DATA BUS
PROGRAM BUS PORT
EXECUTION UNIT
REGISTER SET A
REGISTER SET B
REGISTER SET C
DATA BUS PORT
DATA DATA BUS
PERIPHERAL BUS PORT
PERIPHERAL BUS
VIRTUAL PROCESSOR ARCHITECTURE
PROGRAM ADDR BUS
PROGRAM SHORT ADDRESSING UNIT
ARITHMETIC UNIT
BOOLEAN UNIT
OPERAND BUS A
OPERAND BUS B
RESULT BUS B
DATA SHORT ADDRESSING UNIT
DATA ADDR BUS
PROGRAM DATA BUS
PROGRAM BUS PORT
REGISTER SET A
EXECUTION UNIT
DATA BUS PORT
DATA DATA BUS
SHADOW PROCESSOR A
PROGRAM ADDR BUS
PROGRAM CACHE ADDRESSING UNIT
SHIFT & COMPARE UNIT
BOOLEAN UNIT
OPERAND BUS A
OPERAND BUS B
RESULT BUS B
DUAL DATA SHORT ADDRESSING UNIT
SHARED DATA BUS
DATA ADDR BUS
PROGRAM DATA BUS
PROGRAM BUS PORT
REGISTER SET B
EXECUTION UNIT
SHADOW PROCESSOR B
PROGRAM ADDR BUS
PROGRAM SHORT ADDRESSING UNIT
SHIFT & COMPARE UNIT
DATA SWITCHING UNIT
OPERAND BUS A
OPERAND BUS B
RESULT BUS B
INTERNAL MEMORY BLOCK
PROGRAM DATA BUS
PROGRAM BUS PORT
REGISTER SET A
EXECUTION UNIT
REGISTER SET C
PERIPHERAL INTERFACE
PERIPHERAL BUS
SHADOW PROCESSOR C

FIG. 3

INTERNATIONAL SEARCH REPORT

International Application No
PCT/EP 99/08058

A. CLASSIFICATION OF SUBJECT MATTER
IPC 7 G06F9/38

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 7 G06F

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 5 495 588 A (KNULL KURT ET AL) 27 February 1996 (1996-02-27) column 2, line 35 -column 3, line 18 column 4, line 3 - line 11 column 4, line 56 - line 65 column 5, line 66 -column 6, line 2 ---	1,3-8
X A	GB 1 576 276 A (SIEMENS AG) 8 October 1980 (1980-10-08) the whole document ---	1,3,5,7, 8 4
A	US 5 283 881 A (MARTINI WILLIAM J ET AL) 1 February 1994 (1994-02-01) column 3, line 40 - line 48 --- -/--	2

[X] Further documents are listed in the continuation of box C.

[X] Patent family members are listed in annex.

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Date of the actual completion of the international search	Date of mailing of the international search report
31 January 2000	04/02/2000

Name and mailing address of the ISA	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Tx. 31 651 epo nl, Fax: (+31-70) 340-3016	Moraiti, M

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INTERNATIONAL SEARCH REPORT

International Application No
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